

MEM2310

N-Channel MOSFET MEM2310M3

General Description

MEM2310M3G Series N-channel enhancement mode field-effect transistor ,produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage applications, and low power dissipation in a very small outline surface mount package.

Features

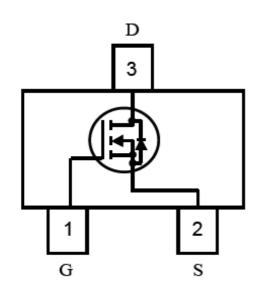
30V/5.8A

$$\begin{split} R_{DS(ON)} = &25m\Omega @~V_{GS} = 10V,~I_D = 5.8A \\ R_{DS(ON)} = &28m\Omega @~V_{GS} = 4.5V,~I_D = 5A \end{split}$$

 $R_{DS(ON)}$ =37m Ω @ V_{GS} =2.5V, I_D =4A

- High Density Cell Design For Ultra Low On-Resistance
- Subminiature surface mount package:SOT23-3L

Pin Configuration



Typical Application

- Battery management
- High speed switch
- Low power DC to DC converter

Absolute Maximum Ratings

| Parameter | | Symbol | Ratings | Unit |
|-------------------------------------|----------------------|------------------|---------|----------------------|
| Drain-Source Voltage | | V_{DSS} | 30V | V |
| Gate-Source Voltage | | V_{GSS} | ±12 | V |
| Drain | T _A =25℃ | 1 | 5.8 | ۸ |
| Current | T _A =70°C | - I _D | 4.9 | A |
| Pulsed Drain Current ^{1,2} | | I _{DM} | 30 | A |
| Total Power | T _A =25℃ | Pd | 1.4 | - W |
| Dissipation | T _A =70°C | Pu | 1 | - vv |
| operating junction temperature | | T _j | 150 | $^{\circ}$ C |
| Storage Temperature Range | | T _{stg} | -65/150 | $^{\circ}\mathbb{C}$ |



Thermal Characteristics

| Parameter | Symbol | TYP. | MAX. | Unit | |
|---|--------------|------|------|------|------|
| Thermal Resistance, Junction-to-Ambient | t≤10s | RθJA | 65 | 90 | °C/W |
| Thermal Resistance, Junction-to-Ambient | Steady-State | RθJA | 85 | 125 | °C/W |
| Thermal Resistance, Junction-to-Lead | Steady-State | RθJL | 43 | 60 | °C/W |

Electrical Characteristics

MEM2310M3

| Parameter | Symbol | Test Condition | Min | Туре | Max | Unit |
|--|---------------------|--|-----|------|------|------|
| | Static (| Characteristics | | | | |
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | V _{GS} =0V, I _D =250uA | 30 | 35 | | V |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D = 250 uA$ | 0.7 | 0.88 | 1.4 | V |
| Gate-Body Leakage | I _{GSS} | $V_{DS}=0V$, $V_{GS}=12V$ | | 0.5 | 100 | nA |
| Gale-Body Leakage | igss | $V_{DS}=0V$, $V_{GS}=-12V$ | | -0.2 | -100 | nA |
| Zero Gate Voltage Drain Current | I _{DSS} | V_{DS} =24V V_{GS} =0V | | | 1000 | nA |
| | R _{DS(ON)} | V_{GS} =10V, I_{D} =5.8A | | 25 | 30 | mΩ |
| Static Drain-Source On-Resistance | | V_{GS} =4.5V, I_{D} =5A | | 28 | 33 | mΩ |
| | | V_{GS} =2.5V, I_D =4A | | 37 | 50 | mΩ |
| Forward Transconductance | g FS | $V_{DS} = 5 \text{ V}, I_{D} = 5 \text{A}$ | 10 | 15 | | S |
| Maximum Body-Diode Continuous Current | ls | | | | 2.5 | Α |
| Source-drain (diode forward) voltage | $V_{\mathtt{SD}}$ | V _{GS} =0V,I _D =1A | | 0.72 | 1.0 | V |
| | Dynamic | Characteristics | | | | |
| Input Capacitance | Ciss | $V_{DS} = 15 V$, | | 823 | 1030 | |
| Output Capacitance | Coss | $V_{GS} = 0 V$, | | 99 | | pF |
| Reverse Transfer Capacitance | Crss | f = 1 MHz | | 77 | | |
| Gate resistance | Rg | V_{GS} =0V, V_{DS} =0V, f =1MHz | | 1.2 | 3.6 | Ω |
| | Switching | g Characteristics | | | | |
| Turn-On Delay Time | td(on) | $V_{DD} = 15 \text{ V},$ | | 7 | 14 | ns |
| Rise Time | tr | $R_L = 2.7\Omega$ | | 15 | 30 | |
| Turn-Off Delay Time | td(off) | $V_{GEN} = 10V,$ $Rg = 3 \Omega$ | | 38 | 76 | |
| Fall-Time | tf | Ng = 5 12 | | 3 | 6 | |
| Total Gate Charge | Qg | $V_{DS} = 15 \text{ V},$ | | 11 | 14.3 | |
| Gate-Source Charge | Qgs | $V_{GS} = 4.5 V$, | | 1.6 | 2.08 | nc |
| Gate-Drain Charge | Qgd | $I_{D} = 5.8A$ | | 2.8 | 3.64 |] |

^{1.} Repetitive rating, pulse width limited by junction temperature.

^{2.} Pulse width <300us, duty cycle <0.5%.



Typical Performance Characteristics

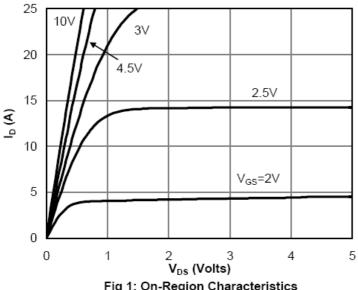


Fig 1: On-Region Characteristics

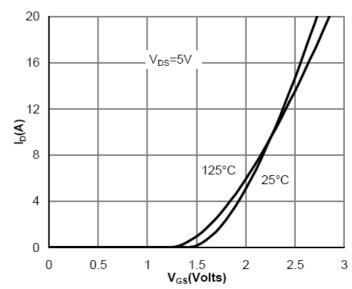


Figure 2: Transfer Characteristics

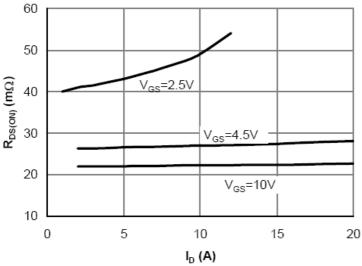


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

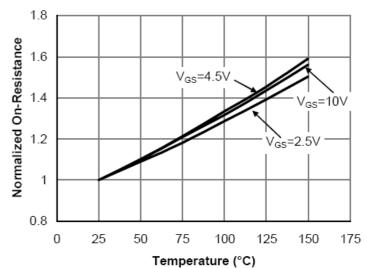


Figure 4: On-Resistance vs. Junction Temperature

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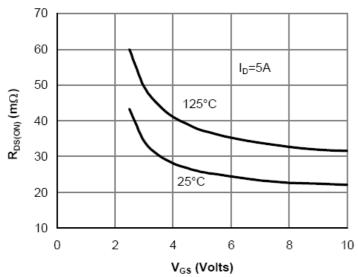


Figure 5: On-Resistance vs. Gate-Source Voltage

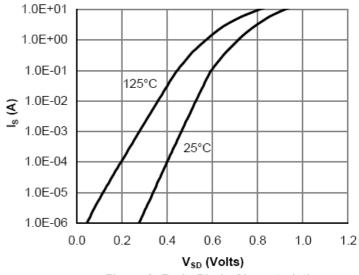


Figure 6: Body-Diode Characteristics

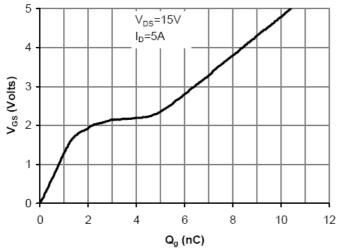


Figure 7: Gate-Charge Characteristics

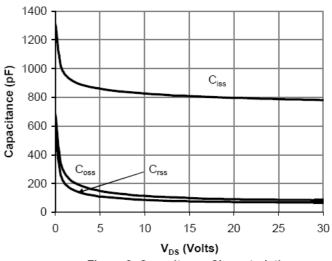


Figure 8: Capacitance Characteristics

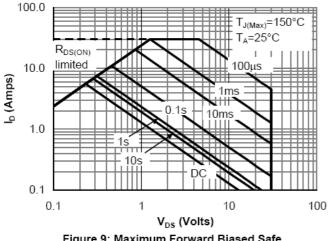


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

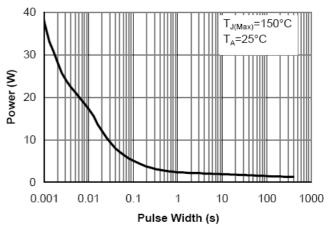


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)



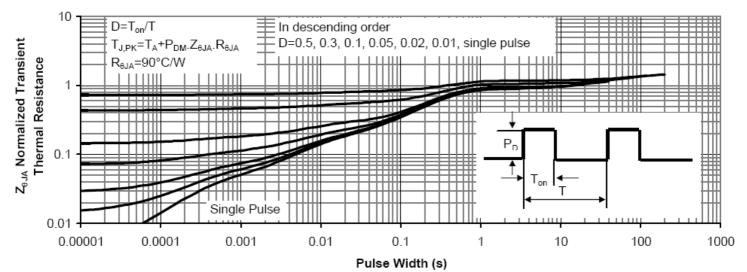
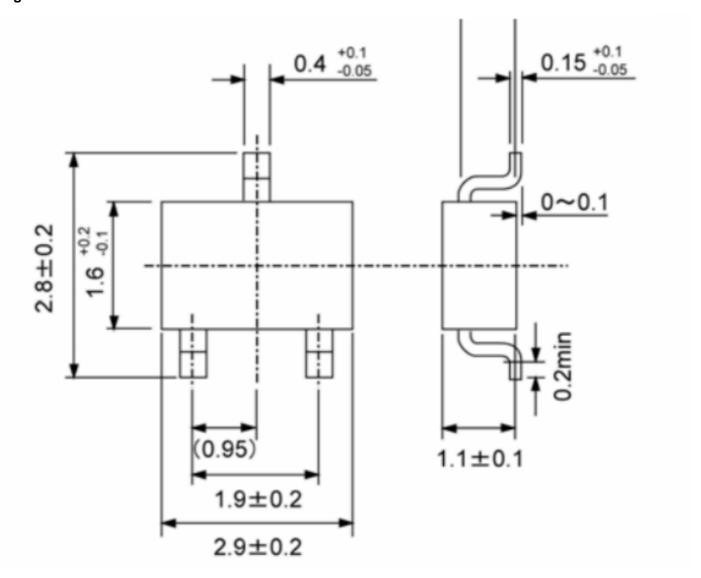


Figure 11: Normalized Maximum Transient Thermal Impedance



Package Information





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