

## P-Channel MOSFET MEM2301X

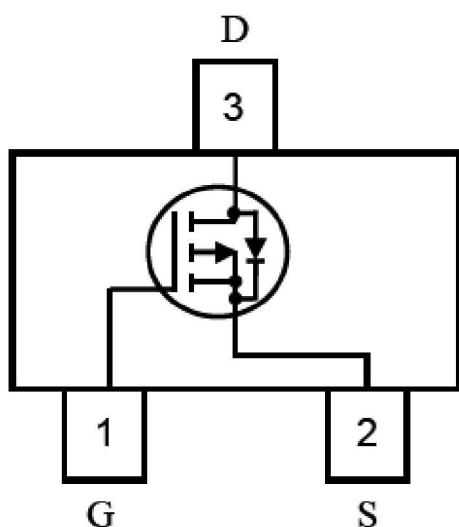
### General Description

MEM2301XG Series P-channel enhancement mode field-effect transistor, produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage applications, and low power dissipation, and low power dissipation in a very small outline surface mount package.

### Features

- -20V/-2.8A  
 $R_{DS(ON)} = 93m\Omega @ V_{GS} = -4.5V, I_D = -2.8A$   
 $R_{DS(ON)} = 113m\Omega @ V_{GS} = -2.5V, I_D = -2A$
- High Density Cell Design For Ultra Low On-Resistance
- Subminiature surface mount package: SOT23

### Pin Configuration



### Typical Application

- Power management
- Load switch
- Battery protection

### Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	$V_{DSS}$	-20	V
Gate-Source Voltage	$V_{GSS}$	$\pm 8$	V
Continuous Drain Current	$I_D$	$T_A = 25^\circ C$	-2.8
		$T_A = 70^\circ C$	-1.8
Pulsed Drain Current <sup>1,2</sup>	$I_{DM}$	-10	A
Total Power Dissipation	$P_d$	$T_A = 25^\circ C$	0.7
		$T_A = 70^\circ C$	0.45
Operating Temperature Range	$T_{Opr}$	150	$^\circ C$
Storage Temperature Range	$T_{stg}$	-65/150	$^\circ C$

## Thermal Characteristics

Parameter	Symbol	MAX.	Unit
Thermal Resistance, Junction-to-Ambient <sup>3</sup>	R $\theta$ JA	145	°C/W

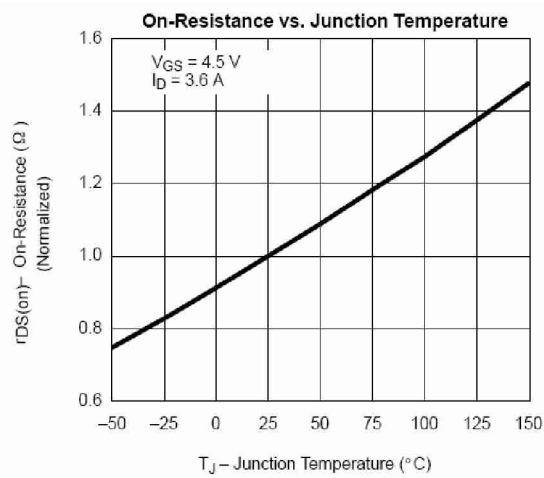
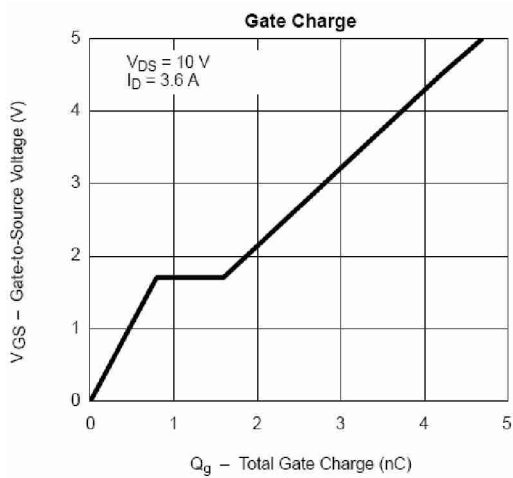
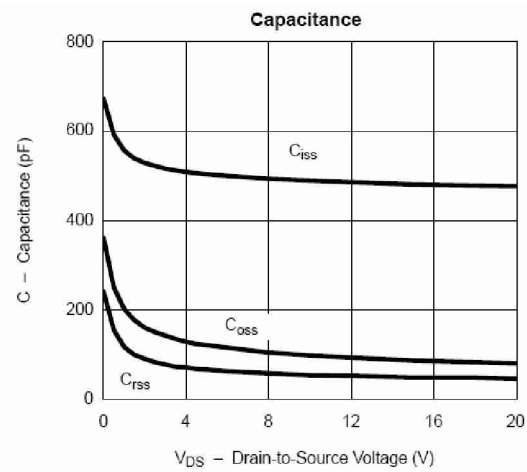
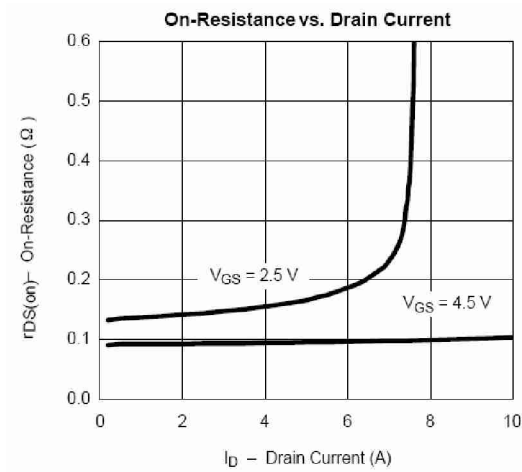
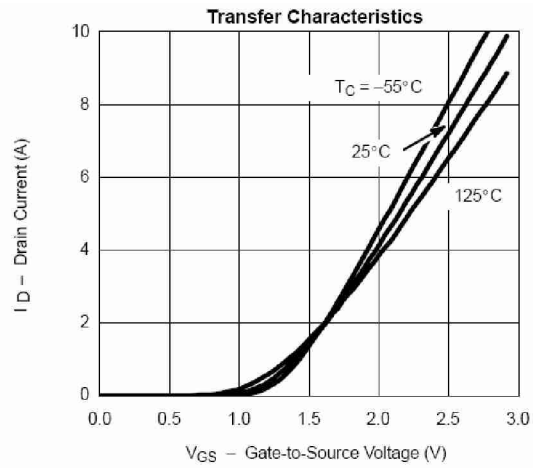
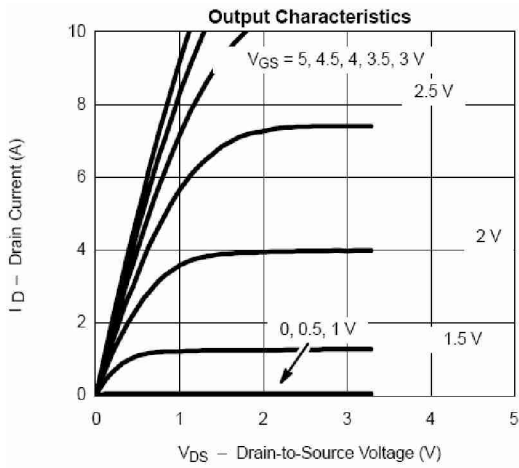
## Electrical Characteristics

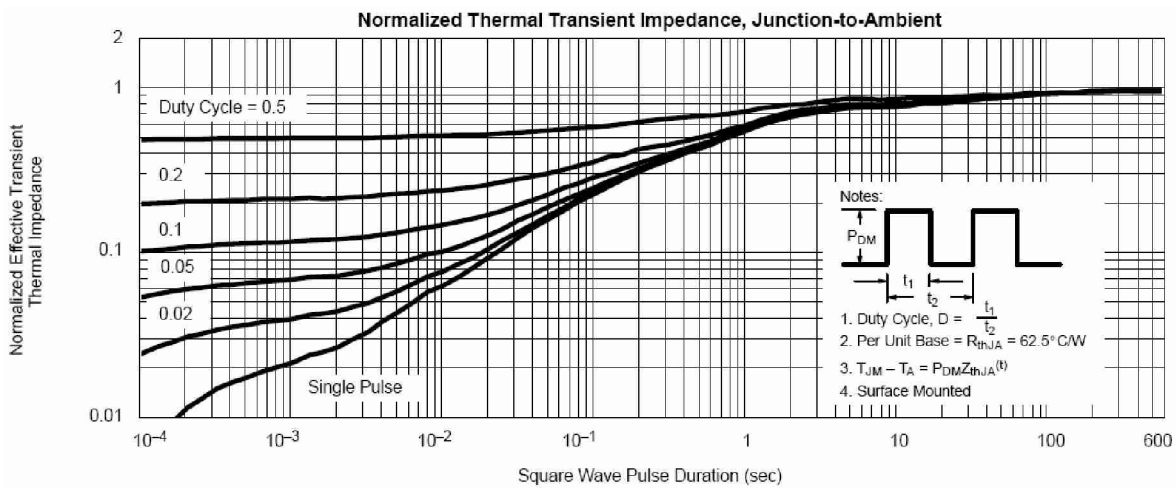
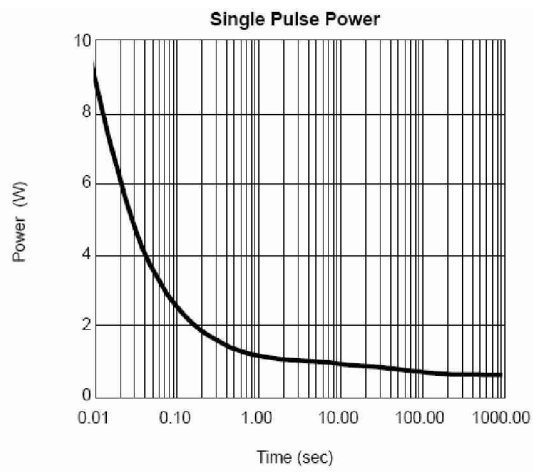
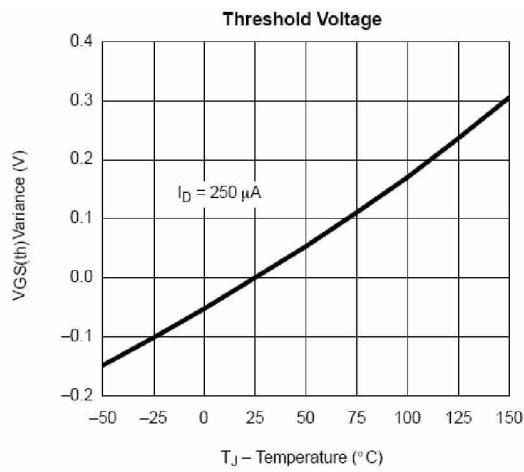
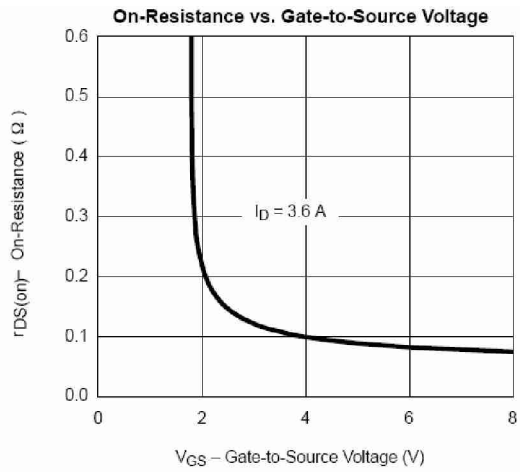
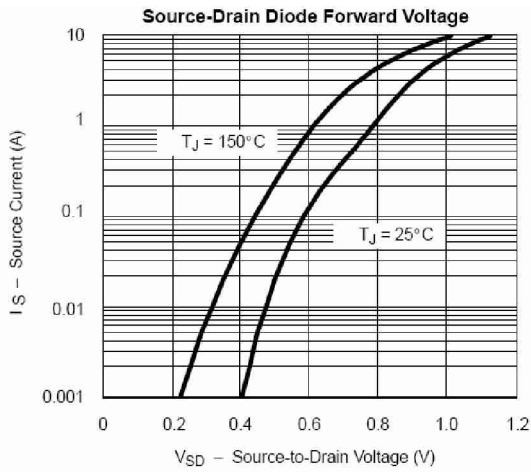
MEM2301XG

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
<b>Static Characteristics</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250 $\mu$ A	-20	-23		V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =-250 $\mu$ A	-0.4	0.58	-1	V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =8V		0.2	100	nA
		V <sub>DS</sub> =0V, V <sub>GS</sub> =-8V		-0.2	-100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-16V V <sub>GS</sub> =0V		-1.5	-100	nA
Static Drain-Source On-Resistance	R <sub>DS(ON)1</sub>	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-2.8A		93	110	m $\Omega$
	R <sub>DS(ON)2</sub>	V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-2A		113	140	m $\Omega$
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = -5 V, I <sub>D</sub> = -2.8 A		6.5		S
Source-drain (diode forward) voltage	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-1A			-1.2	V
<b>Dynamic Characteristics</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -6V, V <sub>GS</sub> = 0 V, f = 1 MHz		500		pF
Output Capacitance	C <sub>oss</sub>			115		
Reverse Transfer Capacitance	C <sub>rss</sub>			60		
<b>Switching Characteristics</b>						
Turn-On Delay Time	td(on)	V <sub>DD</sub> = -6 V, I <sub>D</sub> =-1 A, V <sub>GEN</sub> = -4.5 V, R <sub>g</sub> = 6 $\Omega$		5	25	ns
Rise Time	tr			30	60	
Turn-Off Delay Time	td(off)			25	60	
Fall-Time	tf			10	60	
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = -6 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -2.8A		4.0	10	nC
Gate-Source Charge	Q <sub>gs</sub>			0.8		
Gate-Drain Charge	Q <sub>gd</sub>			0.8		

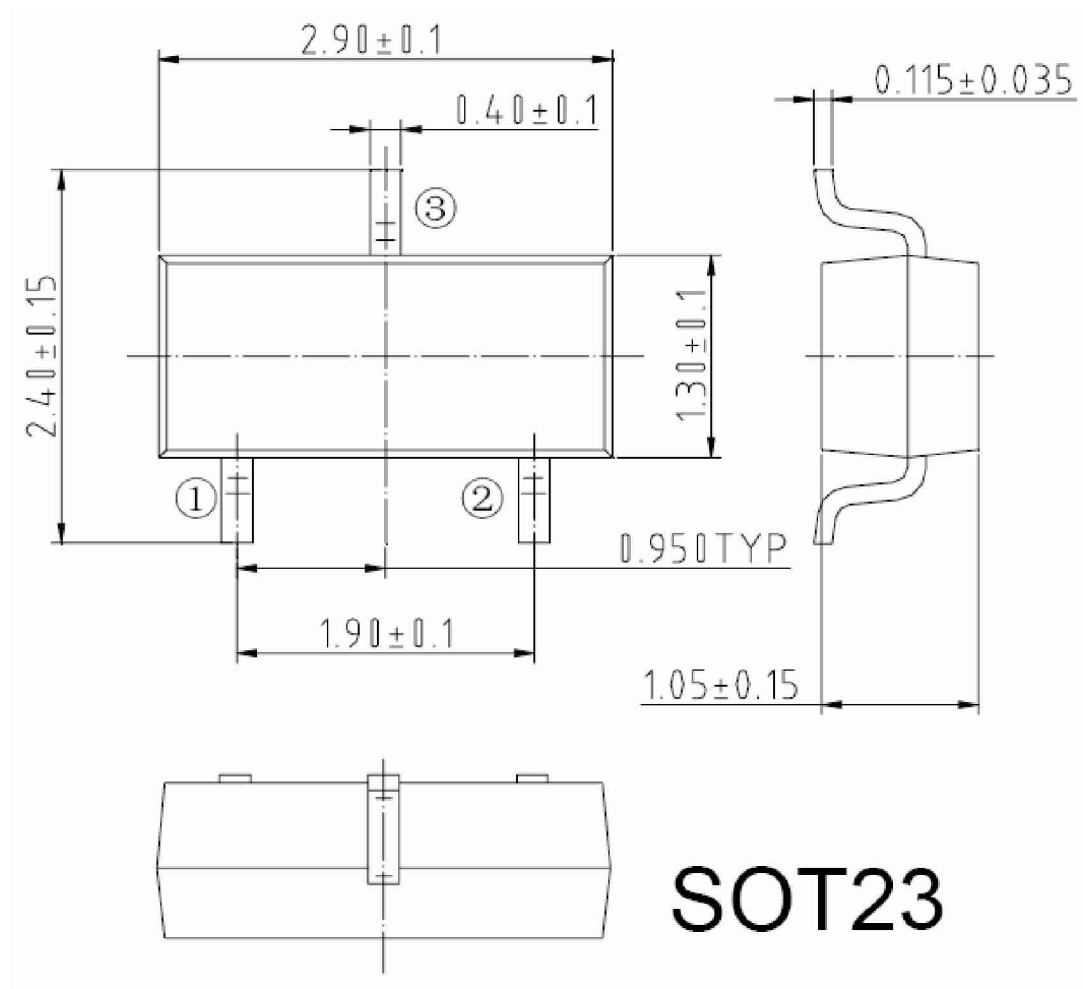
- 1、Pulse width limited by maximum junction temperature.
- 2、Pulse test: PW  $\leq$ 300  $\mu$ s duty cycle  $\leq$ 2%.
- 3、Surface Mounted on FR4 Board, t  $\leq$  5 sec.

## Typical Performance Characteristics





Package Information



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